REMARKS

Applicants respectfully request reconsideration of Examiner's rejection of Claims 2 and 3 under 35 U.S.C. §112. Applicants submit that the use of the term "box-shape" to be fully descriptive of the invention, and its definition to be well known in the art. A search for the term "box shape" returns over 3,500 patents with that term in the specification, and over 500 patents with that term in a claim. See, for example, U.S. Patent No. 6,696,777, which discloses a "box-shape" device in Claim 3 and in Figure 2. In Applicant's invention, the term discloses the rectangular 3-D shape of the semiconductor device assembly jig. For example, in relation to Figure 5a of Applicant's disclosure, it describes the geometric relationship between the walls (33), pins (32), base plate(31), and cover(34) that form a "box-like"3-D rectangular shape. In light of the foregoing, Applicants request that the Examiner withdraw this rejection of claims 2 and 3.

Applicants have amended Claim 6 solely to correct a minor typographical error. Additionally, Applicants have added new claims to alternately define the invention.

Applicants respectfully request reconsideration of Examiner's rejection of Claims 1 – 7 under 35 U.S.C. §102 as being unpatentable over Levy (U.S. Patent No. 5,869,353). Levy is directed to the apparatus of a multi-chip module such that Integrated Circuits (ICs) that fit within a pre-defined aperture of a panel can be bonded together at edges directly to an IC above or below it. Applicants assert this method and device to be entirely distinct from Applicant's currently claimed invention.

For example, Levy discloses a collection 12 of frames 22 to be used in the positioning of semiconductor IC's into pre-defined panel apertures to create a vertically aligned chip package stack. Applicant's invention, however, discloses the use of an assembly jig 3 in the creation of a multi-layered semiconductor device including multiple layers of printed wiring boards and semiconductor ICs. Further, Levy discloses that connections between IC layers be done solely via soldering of the pads 26 and leads 16 on the outside perimeter of the ICs (See Figures 5 and 6). Applicant's invention, however, discloses connections between layers be done via solder bumps 13, and lands 8,9 positioned below or above the printed wiring board or IC (See Figures 2 – 6).

To state it another way, Applicant's current invention would not be in any way applicable to Levy because 1) Levy does not use printed circuit boards between layers that are subject to warping during the reflow step, and 2) Levy requires the dimensions of the semiconductor chips to be within the dimensions of the aperture opening, and therefore does not need to control the height of the device as one does with Applicant's multilayer semiconductor package.

Therefore, Levy provides no teaching or suggestion towards Applicant's currently claimed invention, which provides for an assembly jig to restrict the height of the resulting multi-layered semiconductor module to a consistent and repeatable value, and to suppress deformation due to warp of the layered printed circuit boards. As a result, Applicant's invention improves the yield and productivity in the creation of these multilayer semiconductor devices while incurring minimum additional costs.

In conclusion, and based upon the above amendments and remarks, Applicants respectfully submit that all claims now stand in condition for allowance.

Respectfully submitted,

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